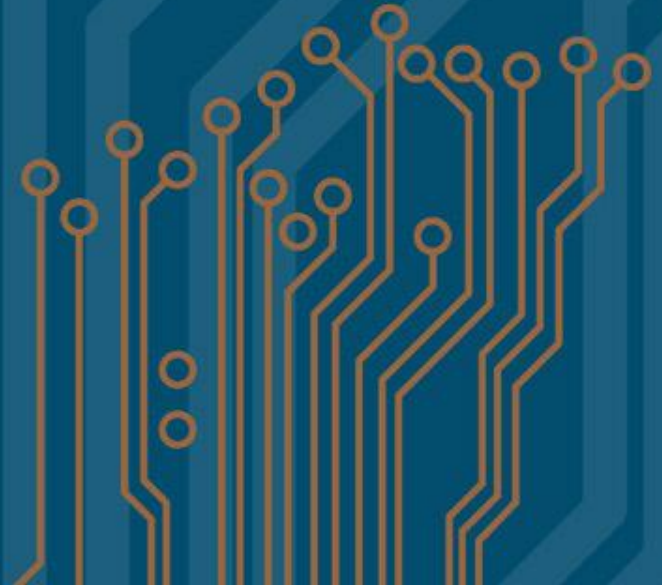




DDi Technology Roadmap PCB & ATE

2011 - 2012



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DDi Technology Roadmap

- **‘DDi Standard’**
DDi’s current everyday capability with no premium.
- **‘DDi Advanced’**
DDi’s current everyday capability with a small premium
- **‘DDi Engineering’** = *DDi has experience with and can fabricate on request with a significant premium; contact DDi engineering to discuss your requirements*
- **‘DDi Development’** = *Process development in-process based on customer demand and collaboration*

PCB Technology Roadmap

Trace & Space

	Standard	Advanced	Engineering	Development
External Trace	0.004"	0.003"	0.0025"	0.002"
External Space	0.004"	0.003"	0.0025"	0.002"
Internal Trace	0.004"	0.003"	0.0025"	0.002"
Internal Space	0.004"	0.003"	0.0025"	0.002"

Drilled Via Size

	Standard	Advanced	Engineering	Development
Drill Diameter	0.010"	0.008"	0.006"	0.004"
Pad Diameter	0.020"	0.016"	0.012"	0.004"

Aspect Ratio

	Standard	Advanced	Engineering	Development
0.006" drill		6.5:1	10:1	14:1
0.008" drill	8:1	10:1	12:1	16:1
0.010" drill	10:1	12:1	16:1	18:1
0.012" drill	10:1	14:1	18:1	20:1
0.0135" drill	10:1	16:1	20:1	24:1

Microvia

	Standard	Advanced	Engineering	Development
Via Diameter	0.006" & 0.005"	0.004"	0.006"	0.004"
Pad Diameter	0.012" & 0.010"	0.008"	0.010"	0.007"
Aspect Ratio	0.6:1	0.8:1	1:1	1:1

2011

2011

2011

2012
2011

PCB Technology Roadmap

		Standard	Advanced	Engineering	Development
Microvia Stack-up	# Microvia layers	1+1	2+2 3+3 4+4	6+6	>7+7
	Buried Sub	Yes	Yes	Yes	Yes
	Stacked MicroVias	No	Yes	Yes	Yes
Microvia Materials	→	Std FR4 Laser Prepregs	Low loss Epoxy Polyimide & BT	Microwave	Film Lased BUM
Attributes	Layer Count Thickness	Up to 24 Up to 0.130"	26 to 44 Up to 0.300"	46 to 60 Up to 0.400"	>60 >0.400"
Laminate Materials	→	High Temp FR4 Lead Free Assembly HDI Flex & Rigid Flex	High Speed Low Loss BT & Polyimide Stablcor	PTFE RF & Microwave	LCP Film Based Non-Reinforced
		2011	2011	2011	2012 2011

PCB Technology Roadmap

		Standard	Advanced	Engineering	Development
Embedded Passives		Buried Capacitance BC2000™	Buried Resistors FaradFlex™ Dupont™ HK-04	High Dk Ceramic Filled	Embedded Active/Passive Devices
Surface Finishes		HASL OSP Immersion Tin	Lead free HASL Immersion Silver Immersion Gold	E-Less Gold Multiple	ENEPIG Neutral Eless Au Ormecon
Solder Mask	Registration				
	Min opening	+/-0.0025" 0.008"	+/-0.002" 0.006"	+/-0.001" 0.005"	<0.001" 0.004"
Via Fill/Cap Plate CVF = Conductive Via Fill Non-CVF = Non-Conductive Via Fill	Min Drilled hole	0.012"	0.010"	0.008"	0.008"
	Aspect ratio	8:1 Non-CVF & CVF	10:1 Non-CVF & CVF	6.5:1 Non-CVF	10:1 Copper CVF
		2011	2011	2011	2012 2011

Current Process Highlights

- **Laser Direct Imaging for improved feature size capability & registration**
- **Reverse Pulse Plating System, current capability up to 20:1 aspect ratio**
- ***FLAT-WRAP™* Technology (wrap plating solution)**
- **Process verification and reliability studies of High Aspect Ratio interconnects with Interconnect Stress Test (IST systems)**
- **Enhanced registration of higher layer count PCBs with the use of vision based tooling systems**
- **Via-in-Pad (Mechanical & Laser drilled microvias)**
- **Stacked MicroVias (SMV®); with solid plated microvias**
- **Laser drilling with UV, UV/CO2, CO2 platforms**
- **Comprehensive metallurgical lab analysis**
- **Controlled impedance tolerance to $\pm 5\%$**
- **Flying probe TDR testing (in-board test capability)**

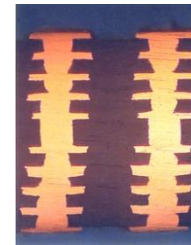
PCB Technology Roadmap

Planned Process Improvements

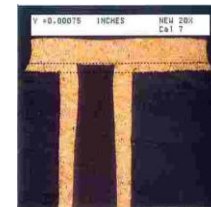
- **Increase Plating Aspect Ratio to >20:1**
- **Reduce Controlled Impedance Tolerance to $<\pm 5\%$**
- **Introduction of advanced plating and photo lithography process**
- **Advanced tooling systems to enable improved registration capability**
- **Continual addition of New Advanced Materials**
- **Continuous evaluation of New Materials for Lead Free Assembly
(245°C - 288° C)**

DDi Enabling Technology

- Laser Drilling Microvia Technology
- Laser Direct Imaging for HDI
- Stacked MicroVias (SMV®) – Solid Copper Plate
- Reverse Pulse Plating – High Aspect Ratio
- *FLAT-WRAP™* Technology (wrap plating solution)
- Flying Probe TDR for Impedance Testing
- Embedded Passives (Capacitance & Resistance)
- Green Materials (Halogen & Lead Free)
- Hybrid Material Construction (PTFE & FR4)
- Thermal Management – Copper Core/STABLCOR®
- NextGen Technology (*NextGen-SMV®*, HDI-Link™, Sub-Link™)
- Solid Copper Via (ThermalVia™)
- Deep Blind Vias (DpBV™)
- Deep Microvias (DpMV™)
- Deep Stacked Microvias (DpSMV®)
- Embedded Heater Circuits (EHC™)



UV/CO2 laser



Robotic TDR



Orbotech LDI
Paragon 8800



DDi Technology Roadmap for Semiconductor Testing

**Automated Test Equipment (ATE)
Burn-In-Boards (BIB)**

Automated Test Equipment (ATE) Burn-In-Boards (BIB)

This market requires special equipment and processing expertise in the following areas:

- **Material movement and layer to layer registration**
- **Lamination process controls**
- **High aspect ratio drilling and positional accuracy**
- **High aspect ratio electroless and electrolytic copper plating**
- **Very tight hole to copper tolerances**

Multiple Levels of Semiconductor Testing

1. Probe Cards



Wafer Level Testing

2. THB Boards



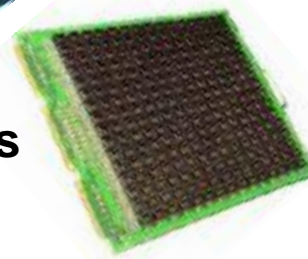
Package Level Testing

3. ATE Boards



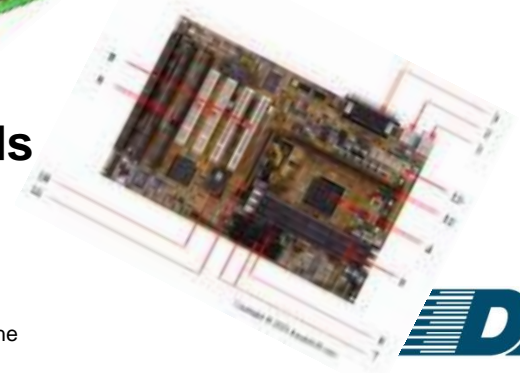
Package Level Testing

4. Burn-in Boards



Package Level Testing

5. System Boards



New Market Opportunities

ATE / BIB Technology Roadmap

- ***'DDi Standard'***
DDi's current everyday capability with no premium.
- ***'DDi Advanced'*** = *DDi's current everyday capability with a small premium*
- ***'DDi Engineering'*** = *product DDi has experience with and can build on request with a significant premium*

ATE / BIB Technology Roadmap

		Standard	Advanced	Engineering
Layer Count	→	Up to 30 layers	32 to 40	42 to 60
Trace & Space	External Trace	0.003"	0.0025"	0.002"
	External Space	0.003"	0.0025"	0.002"
	Internal Trace	0.003"	0.0025"	0.002"
	Internal Space	0.003"	0.0025"	0.002"
Drilled Via Size	Drill Diameter	0.006"	0.006"	0.004"
	Pad Diameter	0.010"	0.008"	0.005"
Aspect Ratio	0.004" drill			32:1
	0.006" drill	20:1	32:1	
	0.008" drill	25:1	32:1	
PCB Thickness	→	0.125" 0.187"	0.200" 0.250"	>0.250"
		2011	2011	2011 - 2012

ATE / BIB Technology Roadmap

		Standard	Advanced	Engineering
Copper Weights	Min Outer	1/2 oz	3/8 oz	1/4 oz
	Min Inner	1/2 oz	3/8 oz	3/8 oz
	Max Inner	1 oz	2 oz	3 & 4 oz
	Max Outer	2 oz	3 & 4 oz	5 oz
Materials	→	Isola 370 HR Nelco 4000-29	N4000-13 EP N4000-13EP SI Polyimide	Rogers 4000
Panel Sizes	→	18" x 24"	16" X 18"	24" x 36"
		21" x 26"	14" X 26"	26" x 30"
		24" x 26"	18" x 30"	
		21" x 24"	24" x 30"	
		2011	2011	2011 - 2012

ATE / BIB Technology Roadmap

	Standard	Advanced	Engineering
Embedded Passives →	BC2000™	FaradFlex™ Dupont HK04	Ceramic Filled
Surface Finishes →	Electrolytic Gold, OSP Lead Free HASL, ENIG Immersion Silver, Immersion Tin	E-Less Gold ENEPIG Multiple Finishes	
Solder Mask Clearance Solder Mask Opening →	+/- 0.0025" 0.008"	+/- 0.002" 0.006"	+/- 0.001" 0.005"
Via Fill/Cap Plate Non-CVF = Non-Conductive Via Fill CVF = Conductive Via Fill →	0.008" Non-CVF & CVF	0.006" Non-CVF & CVF	0.004" Non-CVF
	2011	2011	2011 - 2012

ATE / BIB Technology Roadmap

		Standard	Advanced	Engineering
Drill-to-Copper	→	0.007"	0.006"	0.005"
Min A/R Tangency	→	Drill + 0.008"	Drill + 0.006"	Drill + 0.004"
Circuit to PCB edge	→	0.025"	0.010"	0.008"
Plane to PCB edge	→	0.025"	0.010"	0.008"
Routing Tolerance	→	+/- 0.005"	+/- 0.004"	+/- 0.002"
Edge of hole barrel to PCB Edge	→	0.025"	0.020"	0.016"
Solder Mask Dam	→	0.004" min	0.003" min	0.0025"
		2011	2011	2011 - 2012

ATE / BIB Technology Roadmap

		Standard	Advanced	Engineering
Blind Mechanical Vias	→	0.006"	0.005"	0.004"
Buried Mechanical Vias	→	0.006"	0.005"	0.004"
Laser Drilled Microvias	→	0.006"	0.005"	0.004"
Mechanical Depth Drilled Vias	→	0.5:1	0.75:1	1:1
Back Drill	→	Yes	Yes	Yes
Back Drill Depth Tolerance	→	+/- 0.004"	+/- 0.003"	+/- 0.002"
Stacked Microvias	→	1+1	2+2 3+3	4+4
Copper Filled Microvias	→	Yes	Yes	Yes
Conductive Via Fill Non Conductive Vais Fill	→	Yes Yes	Yes Yes	Yes Yes
Impedance Control	→	+/- 10%	+/- 8%	+/- 5%
Sequential Lamination	→	Yes	Yes	Yes
		2011	2011	2011 - 2012



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